We Claim:

1. An integrated memory, comprising:

a memory cell array, the memory cell array having word lines for selecting memory cells and bit lines for reading out or writing data signals;

a read/write amplifier, the read/write amplifier being connected to the bit lines for assessing and amplifying data signals; and

a voltage generator circuit for generating a voltage supply for application to the read/write amplifier, a potential difference being applied to the read/write amplifier using different supply potentials, the voltage generator circuit increasing the potential difference applied to the read/write amplifier for a limited period of time during an assessment and amplification operation of the read/write amplifier, wherein charge-dependent control is implemented in the voltage generator circuit to generate the increased potential difference using a defined quantity of charge.

2. The integrated memory as claimed in claim 1, wherein the voltage generator circuit increases a first supply potential at a first terminal of the read/write amplifier and/or lowers a second supply potential at a second terminal of the read/write amplifier during an assessment and amplification operation of the read/write amplifier.

3. The integrated memory as claimed in claim 1, wherein the voltage generator circuit has two supply paths for the read/write amplifier, the supply paths having a

different potential difference, the supply paths being driven alternatively to one another in time, the supply paths being connected to the read/write amplifier.

4. The integrated memory as claimed in claim 3, wherein at least two capacitances, the capacitances connected into the supply path which has a higher potential difference, the capacitances being connected to a respective supply potential, the capacitances being connected to the read/write amplifier in the limited period of time, and the capacitances being discharged and charged in this state.

5. The integrated memory as claimed in claim 4, wherein the that supply path which has a higher potential difference is driven by a pulse shaper, which generates a control pulse for the connecting up the capacitances at the beginning of an assessment and amplification operation of the read/write amplifier.